REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated July 22, 2003. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

A copy of the prior art reference US Pat. No. 6,229,513 as described on page 3, lines 10-18 are submitted via the concurrently filed IDS as requested by the Examiner.

Status of the Claims

Claims 1-4 , 7-13 and 17-19 are under consideration in this application. Claims 5-6 and 14 are being cancelled without prejudice or disclaimer. Claims 1-4 and 7-13 are being amended, as set forth above and in the attached marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim Applicants' invention. New claims 17-19 are being added to recite other embodiments described in the specification.

Additional Amendments

The claims and the drawings are being amended to correct formal errors and/or to better disclose or describe the features of the present invention as claimed. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Formality Rejection

Claims 1-14 under 35 U.S.C. § 112, second paragraph, on the grounds of being vague and indefinite. As indicated, the claims have been amended as required by the Examiner. Accordingly, the withdrawal of the outstanding informality rejection is in order, and is therefore respectfully solicited.

Prior Art Rejection

Under 35 U.S.C. § 103(a), claims 1-6 were rejected as being unpatentable over the prior art cited in the present Specification on Page 1, lines 9-12 and Page 3, lines 4-18 (hereinafter "APA"), and in view of JP Pat. No. 04-168417 to Takahara et al. (hereinafter "Takahara"), claims

7-14 were rejected as being unpatentable over the above mentioned prior art and in view of Takahara, and further in view of U.S. Pat. No. 6,424,328 B1 to Ino et al. (hereinafter "Ino"). These rejections have been carefully considered, but are most respectfully traversed.

The liquid crystal display device of the invention (e.g., Figs. 1, 6A), as now recited in claim 1, comprises: a liquid crystal display element 10 with a plurality of drain signal lines D; a plurality of driving circuits 130 including a first driving circuit and a second driving circuit, each of the driving circuits having a plurality of output terminals; and a display control device 110 transmitting display data DATAIN ***alternately*** to one of the output terminals of the first driving circuit and to one of the output terminals of the second driving circuit which is arranged next to the first driving circuit (p. 17, lines 7-13; p. 27, lines 7-13; Fig. 6B: D11 -> D21 -> D12-> D22 -> ... D1n -> D2n ->... D31-> D41-> D32-> D42 ...). At least one of the first and second driving circuits has at least one output terminal being not connected to the drain signal lines (e.g., "*a first drain driver DRV1 has 1 to (n-1) output terminals which are not connected to the drain signal lines*" p. 28, lines 24-27 and Fig. 6A; "*the last drain driver DRV4 has unconnected output terminals*" p. 33, lines 8-12 and Fig. 10; "*the drain drivers DRV1 and DRV2 have unconnected output terminals...[on] arbitrary positions*" p. 34. Lines 12-15 and Fig. 13) and each of the remaining output terminals being connected to one of the drain signal lines. The display control device transmits to said output terminal being ***not connected*** to the drain lines a datum having **a same level** (e.g., Figs. 6B, 12B) as that of a display datum being transmitted prior or subsequently to an output terminal being ***connected*** to one of the drain signal lines, i.e., the **"same-level" feature**.

The present invention, as now recited in claim 3, is also directed to a liquid crystal display device as recited in claim 1, except that the plurality of driving circuits including at least one *odd numbered* driving circuit and at least one *even numbered* driving circuit (rather than just a first and second), and that the even numbered driving circuit is *paired with* and arranged next to the odd numbered driving circuit.

The present invention, as now recited in claims 2 and 4, mirror claims 1 and 3, respectively, but broader to cover all display devices (beyond liquid crystal display devices).

The present invention, as now recited in claim 7 (Fig. 7), is also directed to a liquid crystal display device as recited in claim 3 except (1) not requiring that "the datum transmitted to the output terminal being *not connected* to the drain lines have a same level as that of a display datum being transmitted to an output terminal being *connected* to one of the drain

signal lines"; (2) but requiring that "the display control device has a first storing means 20 ("odd-numbered memory" p. 27, lines 17-21; Fig. 7) for storing display data for said odd numbered driving circuit which are inputted externally and a second storing means 21 ("even-numbered memory") for storing display data for said even numbered driving circuit which are inputted externally, and that the display control device reads out the display data from the first storing means and the second storing means alternately (p. 31, lines 6-12) to transmit to said output terminals being connected to one of the drain signal lines. In particular, before transmitting a display datum D21 to said output terminal being not connected to the drain signal lines (e.g., any one of the terminals 1-(n-1) of DRV1 in Fig. 6A), the display control device 110 reads out from one of said first and second storing means a display datum D21 to be transmitted immediately prior or subsequently to transmitting said display datum to said output terminal being not connected to the drain signal lines (e.g., terminal 1 of DRV2), and then repeatedly transmits said display datum D21 to said output terminal being not connected to the drain signal lines (e.g., terminal 1 of DRV1) and an output terminal being connected to one of the drain signal lines and scheduled to receive said display datum immediately prior or subsequently to the transmitting of said display datum to said output terminal being not connected to the drain signal lines (e.g., terminal 1 of DRV2). For example, in Fig. 6A (p. 32, lines 12-20), "*display data are transmitted in the order of D21, D21, D22, D22, D23, D23...*"("repeating mode") until running out of unconnected output terminals then switching back to "D1n, D2n, $D1n_{+1}$..." ("alternating mode"), i.e., the **"dual-mode" feature**. As such, a plurality of drivers DRV1 to DRVn share a common display control device 110 which includes a pair of memory 20, 21 so as to reduce the cost of the display panel (p. 43, lines 3-5).

Accordingly, "*during transmission of display data containing ineffective display data, it is possible to reduce the transmission frequency on the bus line, whereby it is possible to reduce the amount of generation of radiant electromagnetic noise* (p. 32, last paragraph)".

Applicants respectfully contend that none of the cited references teaches or suggests such a "same-level" or "dual-mode" feature.

Regarding the same-level feature, as admitted by the Examiner (p. 3, third paragraph of the outstanding office action), APA does not show the same level feature. Please also see the attached explanatory charts Fig. A. Takahara merely discloses to skip unused pin, but does not disclose the datum transmitted to the unused pin having the same level as the datum transmitted to the used pin, or the problem of the transmission frequency on the bus line. In addition,

Takahara's display control device simply transmits the display datum to the used pins in the order as the used pins have been physically arranged (i.e., transmitting to all used pins/terminals in DRV 1 but skipping unused pins, then all used pins in DRV 2 but skipping unused pins, etc), rather than ***alternately*** to one of the output terminals of the first driving circuit and to one of the output terminals of the second driving circuit which is arranged next to the first driving circuit (i.e., transmitting to all terminals without skipping. In other words, terminal 1 of DRV1-> terminal 1 of DRV2-> terminal 2 of DRV1-> terminal 2 of DRV2-> ... terminal n of DRV1-> terminal n of DRV2->... terminal 1 of DRV3-> terminal 1 of DRV4-> ...). Please see the attached explanatory charts Fig. B.

Therefore, Takahara not only fails to disclose the same-level feature, but also *teaches away* from the invention (transmitting data with a same level to a non-connected terminal/pin) by skipping (not transmitting any signals to) the unused/unconnected pins/terminals. It is well established that a rejection based on cited references having principles that teach away from the invention is improper.

Contrary to the Examiner's allegation that "it is obvious to one of ordinary skill in the art at the time of invention that ineffective datum will have the same level between and of one ST pulse and start of the another as that of an effective display datum being transmitted prior as shown by Takahara in APA apparatus even when the output bit number of a driver IC is larger than the circuit number of the divided electrode groups (p. 3, last paragraph of the office action)," one skilled in the art will not be motivated to combine APA (transmitting data with a different level to a non-connected terminal/pin) and Takahara (skipping unused pins) as suggested by the Examiner since APA and Takahara teach away from each other. It is well established that a rejection based on cited references having contradictory principles is improper.

Even if, arguendo, a person of ordinary skill were motivated to combine the teachings in Takahara and APA, such combined teachings would still fall short in fully meeting the Applicants' claimed invention as set forth in claims 1-4 since, as discussed, there is no teaching of the same-level feature in either Takahara or APA.

In addition, the Examiner's reliance upon the "common knowledge and common sense" of one skilled in the art for the allegedly obviousness and any motivation for combining the teachings in APA and Takahara did not fulfill the agency's obligation to cite references to support its conclusions. Instead, the Examiner must provide the specific teaching of allegations of obviousness or motivation to combine on the record, such as *statements in the prior art*, to

allow accountability.

> *To establish a prima facie case of obviousness, the Board must, inter alia, show "some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). "The motivation, suggestion or teaching may come explicitly from* ***statements in the prior art****, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved." Kotzab, 217 F.3d at 1370, 55 USPQ2d at 1317. .... Recently, in In re Lee, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002), we held that the Board's reliance on "common knowledge and common sense" did not fulfill the agency's obligation to cite references to support its conclusions. Id. at 1344, 61 USPQ2d at 1434. Instead, the Board must document its reasoning on the record to allow accountability. Id. at 1345, 61 USPQ2d at 1435.*
>
> See In re Thrift, 298 F.3d 1357.

Such an obligation to provide specific teaching(s) also applies to other existing or future obviousness rejections.

Regarding the dual-mode feature, as admitted by the Examiner (p. 7, 3rd paragraph of the outstanding office action), APA and Takahara do not show "a first storing means for storing display data for said odd numbered driving circuit which are inputted externally and a second storing means for storing display data for said even numbered driving circuit which are inputted externally and that the display control device reads out the display data from the first storing means and the second storing means alternately to transmit to the driving circuits".

Ino was relied upon by the Examiner to compensate for such deficiencies. However, Ino (Fig. 15) merely discloses a pair of memory 672n, $672n_{+1}$ ... corresponding to a pair of drivers, rather than a pair of memory 20, 21 ... shared by a plurality of drivers DRV1 to DRVn as recited in claims 7 and 10. Please see the attached explanatory charts Fig. C.

Ino fails to disclose "reading out the display data from the first storing means and the second storing means alternately to transmit to said output terminals being connected to one of the drain signal lines" (the alternating mode). Nor does Ino disclose "reading out from one of said first and second storing means a display datum D21 to be transmitted immediately prior or subsequently to transmitting said display datum to said output terminal being not connected to the drain signal lines (e.g., terminal 1 of DRV2), and then repeatedly transmits said display datum D21 to said output terminal being not connected to the drain signal lines (e.g., terminal

1 of DRV1) and an output terminal being connected to one of the drain signal lines and scheduled to receive said display datum immediately prior or subsequently to the transmitting of said display datum to said output terminal being not connected to the drain signal lines (e.g., terminal 1 of DRV2)" (the repeating mode). According, Ino doesn't teach the dual-mode feature. Accordingly, the present invention as now recited in all the claims is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicant respectfully contends that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

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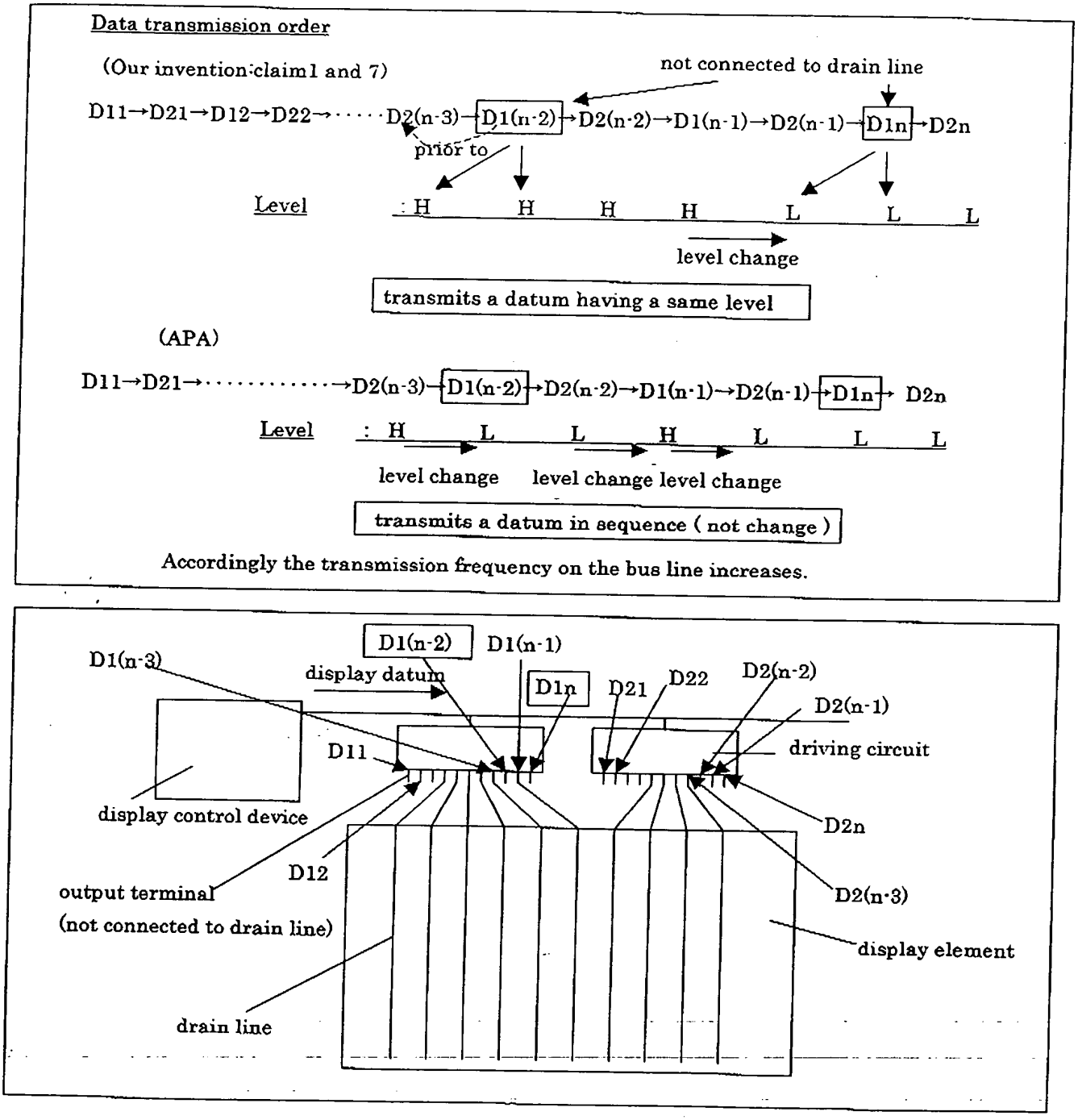
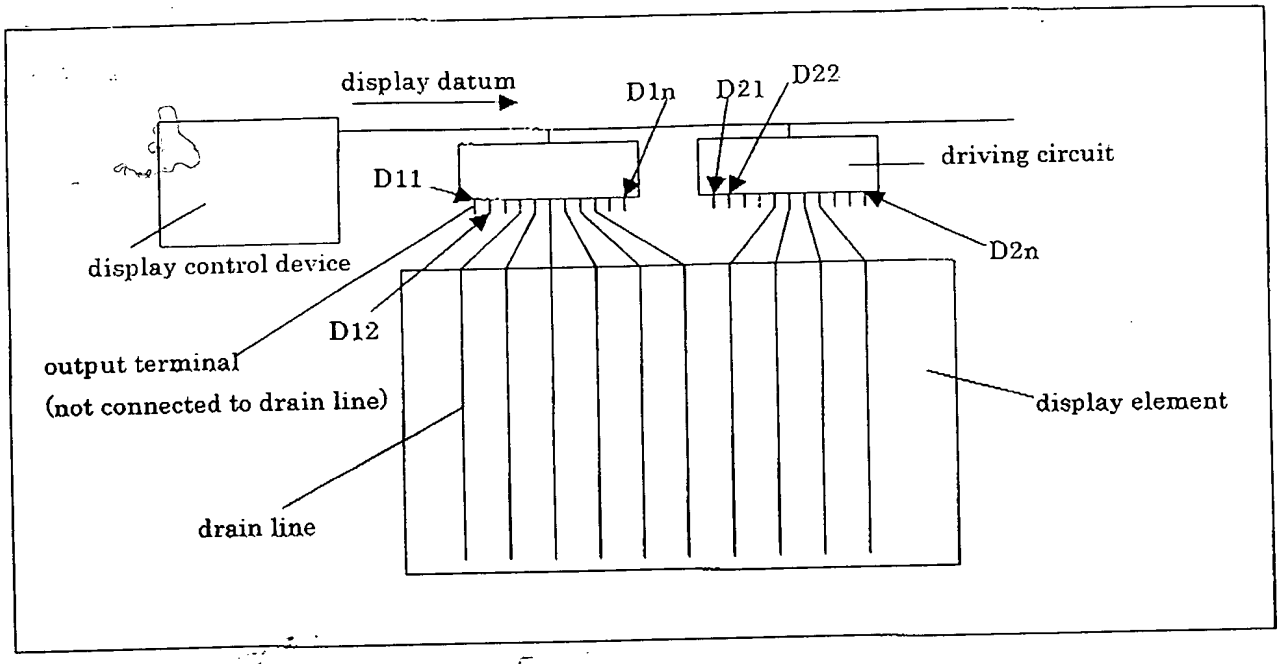
SPF/JCM/JT


Data transmission order
(Our invention:claim1 and 7)
not connected to drain line
D11→D21→D12→D22→·····D2(n-3)→D1(n-2)→D2(n-2)→D1(n-1)→D2(n-1)→D1n→D2n
prior to
Level
: H H H H L L L
level change
transmits a datum having a same level
(APA)
D11→D21→·····→D2(n-3)→D1(n-2)→D2(n-2)→D1(n-1)→D2(n-1)→D1n→ D2n
Level
: H L L H L L L
level change
level change level change
transmits a datum in sequence (not change)
Accordingly the transmission frequency on the bus line increases.

D1(n-2)
D1(n-1)
D1(n-3)
display datum
D1n
D21
D22
D2(n-2)
D2(n-1)
D11
driving circuit
display control device
D2n
D12
output terminal
(not connected to drain line)
D2(n-3)
display element
drain line

Fig. A



Data transmission order

(Our invention)

not connected to drain line

D11→D21→D12→D22→···→D18→D28→···→D2(n-2)→D1(n-1)→D2(n-1)→D1n→D2n

prior to　subsequently to

transmits a datum having a same level

(Takahara)

D11→D12→D13→···→D1(n-2)→D1(n-1)、D1n→D21→D22→···→D2n

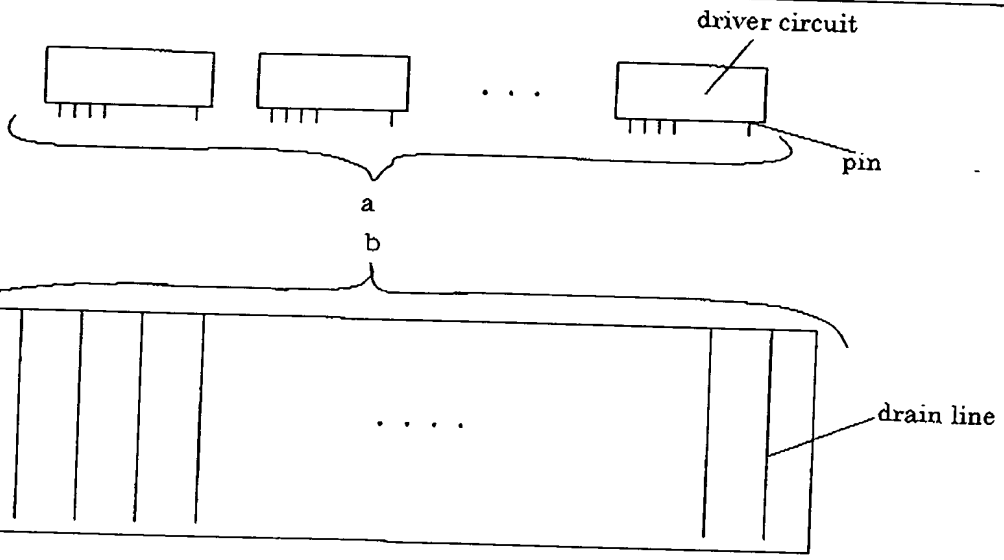
skip (if D1(n-1)、D1n are not connected to drain line)

Fig. B

As to Ino

Our invention differs from the precondition of Ino. And all of the pin in Ino are connected the drain lines (although Ino uses time-division driving).

In addition, SAMPLING CIRCUIT (671n) of Fig.15 in Ino is a simply sampling circuit. And the SAMPLING CIRCUIT (671n) is not included in the display control device like our invention but included in the driver circuit.



The number of the driver's pin =a

The number of the drain line =b

Our invention, APA, and Takahara : a>b

Ino : a<b

Accordingly Ino is not related to our invention and cannot be combined other Prior Art.

Fig.C